

**In the Claims**

Please replace all prior versions, and listings, of claims in the application with the following listing of claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing:

**Listing of Claims**

1. (Original) A processing system for accessing first and second data types, the first data type being data supplied from a peripheral and the second data type being randomly accessible data held in a data memory, the processing system comprising:

a processor for executing instructions;

a stream register unit connected to supply data from the peripheral to the processor;

a FIFO connected to receive data from the peripheral and connected to the stream register unit by a communication path, along which the said data can be supplied from the FIFO to the stream register unit; and

a memory bus connected between the data memory and the processor, across which the processor can access the randomly accessible data.

2. (Original) A processing system according to claim 1, wherein the stream register unit forms part of the processor.

3. (Original) A processing system according to claim 1, wherein data is supplied from the FIFO to the stream register unit in accordance with requests for data made by the processor to the stream register unit and forwarded to the FIFO.

4. (Original) A processing system according to claim 3, wherein the said requests are made as accesses to volatile variables.

5. (Original) A processing system according to claim 3, wherein the FIFO is arranged to, upon receiving a request for data from the stream register unit, send a signal to the

stream register unit indicating availability of the requested data.

6. (Original) A processing system according to claim 5, wherein if the FIFO contains the requested data, the said signal to the stream register unit indicates that the data is available, and the FIFO is further arranged to send a signal to the stream register unit comprising the data.

7. (Original) A processing system according to claim 6, wherein the stream register unit is arranged to, following receipt of the signal comprising the data, supply the data to the processor.

8. (Original) A processing system according to claim 6, wherein the stream register unit is arranged to, following receipt of the signal comprising the data, send a signal to the FIFO indicating that it has taken the data.

9. (Original) A processing system according to claim 8, wherein the said signal to the FIFO further indicates the next location in the FIFO from which data is required.

10. (Currently Amended) A processing system according to ~~any of~~ claim 5, wherein the FIFO is further arranged to, if it does not contain the requested data, send a different signal to the stream register unit indicating that the data is not available.

11. (Original) A processing system according to claim 10, wherein the stream register unit is arranged to, if the signal sent by the FIFO is the said different signal indicating that the data is not available, send a stall signal to the processor, causing the processor to stop executing instructions.

12. (Original) A processing system according to claim 10, wherein the FIFO is further arranged to, if following sending of the said different signal to the stream register unit the

data subsequently becomes available, send a signal to the stream register unit indicating that the data is available, and to send a signal comprising the data to the stream register unit.

13. (Currently Amended) A processing system according to ~~any~~ of claim 5, further comprising a timeout generator, arranged for communication with the processor and the stream register unit, and arranged to, if the signal sent by the FIFO is the said different a signal indicating that the data is not available, after a predetermined period of time, send a timeout signal to the processor, causing the processor to interrupt such that it can execute other instructions.

14. (Original) A processing system according to claim 13, wherein if following sending of the timeout signal to the processor the data subsequently becomes available, the timeout generator is arranged to receive a signal instructing it to cease sending the timeout signal, and to, upon receipt of the said instruction, cease sending the timeout signal.

15. (Original) A processing system according to claim 13, wherein the stream register unit is arranged to, if following sending of the timeout signal to the processor the data subsequently becomes available, send the data to the processor.

16. (Original) A processing system according to claim 1, wherein the stream register unit is associated with a register file containing a plurality of registers and a load/store unit arranged to receive data from the stream register unit and temporarily store the data in the register file.

17. (Original) A processing system according to claim 16, wherein the processor is arranged to retrieve data from the register file.

18. (Original) A processing system according to claim 1, wherein data is supplied from the FIFO to the stream register unit in accordance with requests for data made by the

processor to the stream register unit and forwarded to the FIFO, wherein the stream register unit is associated with a register file containing a plurality of registers and a load/store unit arranged to receive data from the stream register unit and temporarily store the data in the register file, wherein the processor is further arranged to make requests for data to the stream register unit via the load/store unit.

19. (Currently Amended) A processing ~~unit~~ system according to claim 1, wherein the stream register unit comprises one or more FIFOs connected to receive data from the FIFO connected to the stream register and supply the data to the processor.

20. (Original) A processing system according to claim 3, wherein the request for data is a request for a single data item.

21. (Original) A processing system according to claim 1, further comprising one or more additional FIFOs linked together between the said FIFO and the communication channel.

22. (Original) A processing system according to claim 1, wherein the data from the peripheral is video data.

23. (Currently Amended) A processing system according to claim ~~23~~ 22, wherein the peripheral is a video processing system.

24. (Original) A streaming data handling system, comprising :  
a processor;  
a stream register associated with the processor;  
a FIFO memory connected to the processor via the stream register,  
wherein the stream register and the FIFO operate the same data handling protocol such that the stream register can receive streamed data items from the FIFO memory and supply them to the processor in the received order.

25. (Currently Amended) A system according to claim 24, further comprising a timeout generator, arranged for communication with the processor and the stream register, and arranged to, if the signal sent by the FIFO is ~~the said different~~ a signal indicating that the data is not available, after a predetermined period of time, send a timeout signal to the processor, causing the processor to interrupt such that it can execute other instructions.

26. (Original) A stream register connectable between a processor and a peripheral, the stream register comprising :

a receiver arranged to receive a request for a data item from the processor; and

a stream engine, arranged to send the request to the peripheral and receive one or more signals back from the peripheral indicating availability of the requested data item, and, if the data item is available, send the data item to the processor and if the data item is not available, send a timeout signal to the processor.

27. (Original) A stream register according to claim 26, wherein the stream engine is arranged to the interrupt signal to the processor after a predetermined period of time.

28. (Original) A stream register according to claim 27, wherein the stream engine is further arranged to, if the data is available, temporarily store the data in a register file for access by the processor.

29. (Original) A stream register according to claim 27, wherein the stream engine is further arranged to, following sending of the timeout signal to the processor, if the data item subsequently becomes available, receive a signal instructing it to cease sending the timeout signal, and to, upon receipt of the said instruction, cease sending the timeout signal to the processor and temporarily store the data in a register file for access by the processor.

30. (Original) A stream register connectable between a processor and a memory, the

stream register comprising :

a receiver arranged to receive a request for a data item from the processor; and  
a stream engine, arranged to send the request to the memory and receive one or more signals back from the memory indicating availability of the requested data item, and, if the data item is available, send the data item to the processor and if the data item is not available, send a stall signal to the processor.